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10/806,128	03/23/2004	Hiroshi Ogasawara	ASAM.0116	2109

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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,128	OGASAWARA ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/22/04,02/01/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination in this application (10,806,128) filed on March 23, 2004.

Claims 12-20 have been withdrawn.

Claim 1 has been amended.

Acknowledgement is made to the Information Disclosure Statement received on November 22, 2004, February 1, 2005, and April 19, 2005.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunphy et al. (US 5,077,736), in view of Belsan (US 5,155,835), and further in view of Yamamoto (US Patent Application Publication 2002/0152339).

It should be noted that the inventions disclosed by Dunphy et al. and Belsan are assigned to the same assignee (Storage technology Corporation, Louisville, Colorado) and teach different aspects of the same data storage system. Therefore, no further explanation, justification or motivation is considered necessary, and will not be provided by the examiner, for the combination of the two inventions to serve as the ground of the following claim analysis.

As to claim 1, Dunphy et al. and Belsan disclose **a disk array system** [Dunphy et al., Disk Drive Memory (title); Belsan, Multilevel, Hierarchical Dynamically Mapped Data Storage Subsystem (title)] **comprising**:

a plurality of storage devices for storing data [Dunphy et al., a plurality of disk drives (figure 1, 130-0~130-M)];

a storage device control unit for controlling storage of data in said plurality of storage devices [Dunphy et al., figure 1, the storage control device comprising control modules (101~104); disk drive manager; and directors (151~154); figures 2-4],

a connection unit being connected with said storage devices [Dunphy et al., the corresponding connection unit comprising the cross point switches (figure 1, 121~124); the plurality of disk drives are switchably interconnectable (column 2, lines 58-60)];

a plurality of first channel control units [Dunphy et al., figure 1, control modules 101~104; figure 3] **each having a first processor of converting file data** [Dunphy et al., control processor, figure 3, 301; Blesan, this ensures that the data files received from the host processor are distributed across the plurality of disk drives (column 17, lines 26-30)], **received through an local area network outside said disk array system itself** [Dunphy et al., via the central processing unit as shown in figure 1, 150] **into block data** [Belsan, figure 5, the ESDI control unit deals with block data complying to the ESDI data standard] **and requiring storage of said data in said plurality of storage devices** [Dunphy et al., figure 1; column 9, lines 60-68; column 10, lines 1-50] **and a second processor** [Dunphy et al., the corresponding second processor is the processor (figure 4, 401) residing in the disk drive manager (figure 1,

140)] **of transferring said block data to said plurality of storage devices through said connection unit and said storage device control unit in response to said request sent from said first processor** [Dunphy et al., column 12, lines 55-68; column 13, lines 1-55], **and said plurality of first channel control units being connected with said connection unit** [Dunphy et al., figure 1, 121~124] and said **local area network** [Dunphy et al., via the central processing unit as shown in figure 1, 150; Belsan, via the host processors (figure 1, 11 and 12)];

a shared memory for storing control information to be transferred between said plurality of first channel control units and said storage device control unit [Dunphy et al., the corresponding shared memory is the cache memory (figure 2, 203) connected between the control processor (figure 2, 202) and the disk controller (figure 2, 204)]; **and**

a cache memory for temporarily saving data to be transferred between said plurality of first channel control units and said storage device control unit [Dunphy et al., the corresponding cache memory is the cache memory shown in figure 2, 203]; **and**

wherein said second processor located in each said plurality of first channel control units divides a plurality of storage areas in said plurality of storage devices for storing said block data [Dunphy et al., figure 5; column 11, lines 46-68; column 12, lines 1-54] **and a processor information storage area for storing processor information regarding a processing state of each of said first processors to be transferred among said plurality of said first processors**

through the use of said plurality of storage areas of said storage devices [Dunphy et al., the history log, figure 4, 404; column 13, lines 10-55], **and aid storage device control unit copies said processor information stored in said processor information storage area into a backing up storage area** [Dunphy et al., the specific information of which physical disk are contained in a redundancy group is stored in a local memory and a copy of that information is transmitted to each of the control modules (column 13, lines 19-55)].

Regarding claim 1, Dunphy et al. and Belsan do not explicitly mention **connection to a local area network**. However, Dunphy et al. and Belsan do teach the presence of a host processor associated with the storage system, which facilitates the connection to an external network. Further, it is well known in the art how a local area network function (see Microsoft Computer Dictionary, 5th edition, 2002, Microsoft Press, page 315 – local area network) and what it takes to connect a host processor to a local area network. Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the common and ordinary nature of the use of a local area network, hence lacking patentability.

Regarding claim 1, Dunphy et al. and Belsan do not explicitly mention **converting file data into block data**. However, Yamamoto teaches in the invention "Direct Access Storage System with Combined Block Interface and File Interface Access" a storage system with combined block interface and block interface. In particular, a NFS interface adaptor (figure 1, 28) is in place to convert the file interface information of the request to block interface information and to pass the block interface

information to a disk drive (paragraph 0029). A file interface adaptor allows the file data to be received directly from sources operated using file format, such as the Internet, and stored in the disk drive. Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the benefits of a file interface adaptor, as demonstrated by Yamamoto, and to incorporate into the existing scheme disclosed by Dunphy et al. and Belsan to further improve the flexibility and inter-operability of the storage system.

As to claim 2, Dunphy et al. and Belsan teach that **the first processor located in each of said plurality of first channel control units indicates storage of information about the processing status of said first processor to said second processor located in said first channel control unit provided with said first processor** [Dunphy et al., the specific information of which physical disk are contained in a redundancy group is stored in a local memory and a copy of that information is transmitted to each of the control modules (column 13, lines 19-55)], **and said second processor located in said first channel control unit provided with said first processor controls storage of the information about the processing status of said first processor in said processor information storage area in response to an indication given from said first channel control unit** [Dunphy et al., when a request for a specific piece of information is received by the control modules from a storage director ... (column 13, lines 19-55)].

As to claim 3, Dunphy et al. and Belsan teach that **the second processor located in each of said plurality of first channel control units saves said block**

data in said cache memory [Belsan, cache memory, figure 2, 113; the data is written into, for example, cluster controller which stores the data in cache (column 6, lines 1-23)] **and stores information for representing saving of said block data in said cache memory in said shared memory** [Dunphy et al., the corresponding shared memory is the cache memory (figure 2, 203) connected between the control processor (figure 2, 202) and the disk controller (figure 2, 204); Belsan, figures 8-9] **in response to a request given from said first processor located in said first channel control unit provided with said second processor** [Dunphy et al., the specific information of which physical disk are contained in a redundancy group is stored in a local memory and a copy of that information is transmitted to each of the control modules (column 13, lines 19-55)], **and**

said shared memory is caused to store said information for representing saving of said block data in said cache memory under the control of said second processor located in each of said plurality of first channel control units [Belsan, figures 8-13; column 9, lines 45-50].

As to claim 4, Dunphy et al. and Belsan teach that **the first processor located in each of said plurality of first channel control units indicates said storage device control unit to copy said information' stored in said processor information storage area to the storage area for backing up said processor information** [Dunphy et al., the specific information of which physical disk are contained in a redundancy group is stored in a local memory and a copy of that information is transmitted to each of the control modules (column 13, lines 19-55); a

pool of backup disk drives are allocated to replace a failed disk drive (column 3, lines 3-25)], **and**

said storage device control unit controls a copy process in response to an indication given from said first processor [Dunphy et al., when a request for a specific piece of information is received by the control modules from a storage director ... (column 13, lines 19-55); Belsan, in additional to having a copy stored on the plurality of disk drives (column 14, lines 59-68)].

As to claim 5, Dunphy et al. and Belsan teach that **the first processor located in each of said plurality of first channel control units reads or writes the information** [Belsan, Data Read Operation, column 14, 45-68; column 15, lines 1-16; Data Write Operation, column 16, lines 36-68; column 17, lines 1-56] **stored in said storage area for backing up said processor information** [Belsan, a reliability improvement is obtained by providing a pool of disk drives as backup (column 6, lines 25-45)], **thereby keeping the process if the read or the write of said information stored in said processor information storage area is disabled** [Belsan, the backup disk drive is switched over to replace a failed disk drive (column 6, lines 25-45); Dunphy et al. a pool of backup disk drives are allocated to replace a failed disk drive (column 3, lines 3-25)].

As to claim 6, Dunphy et al. and Belsan teach that **plurality of first channel control units are classified into a plurality of cluster groups** [Belsan, the cluster control, figure 1, 111 and 112], **said processor information storage area** [Dunphy et al., the history log, figure 4, 404; column 13, lines 10-55] **includes a plurality of**

processor information storage portions, and each different one of said plurality of processor information storage portions is allocated to the corresponding one of said plurality of cluster groups [refer to "As to claim 1"].

As to claim 7, Dunphy et al. and Belsan teach that **the plurality of first channel control units included in the first one of said plurality of cluster groups** [Belsan, the cluster control, figure 1, 111, is the first cluster group] **are caused to store information about the processing status between said first processors in the first one of said plurality of processor information storage portions** [Dunphy et al., the specific information of which physical disk are contained in a redundancy group is stored in a local memory and a copy of that information is transmitted to each of the control modules (column 13, lines 19-55)], **and**
said plurality of first channel control units included in the second one of said plurality of cluster groups [Belsan, the cluster control, figure 1, 112, is the second cluster group] **are caused to store information about the processing status between said first processors in the second one of said plurality of processor information storage portions** [Dunphy et al., the specific information of which physical disk are contained in a redundancy group is stored in a local memory and a copy of that information is transmitted to each of the control modules (column 13, lines 19-55)].

As to claim 8, Dunphy et al. and Belsan teach that **the first processor of each of said plurality of first channel control units included in said first cluster group**

indicates creation of duplication of information stored in said first processor information storage portion to said storage device control unit, and said storage device control unit is caused to store duplication of the information stored in said first processor information storage portion in a first backup area included in said storage area for backing up said processor information in response to an indication of said first processor of said plurality of first channel control units included in said first cluster group [Belsan, a reliability improvement is obtained by providing a pool of disk drives as backup (column 6, lines 25-45); the backup disk drive is switched over to replace a failed disk drive (column 6, lines 25-45); Dunphy et al. a pool of backup disk drives are allocated to replace a failed disk drive (column 3, lines 3-25)].

As to claim 9, refer to "As to claim 8."

As to claim 10, refer to "As to claim 8."

Also regarding claim 10, Dunphy et al. and Belsan do not explicitly mention **the use of a management terminal for obtaining information about the storage system**. However, Dunphy et al. and Belsan do teach the presence of a host processor associated with the storage system. However, it is well known in the art that the host processor unit is usually equipped with a terminal with keyboards and monitors so that human operators can interactively participate in the control of the operations of the system. Further, Yamamoto specifically teaches the using of a administrator terminal interface (figure 1, 43) to allow interactive participation from a system operator. Therefore, it would have been obvious for one of ordinary skills in the

art at the time of Applicants' invention to recognize the common and ordinary nature of the use of a management terminal, hence lacking patentability.

As to claim 11, refer to "As to claim 5."

4. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Fujimoto et al., (US 6,385,681), "Disk array Control Device with Two Different Internal Connection Systems."
- Kanda et al., (US 6,115,797), "Method and System for Sharing Storage Device via Mutually Different Interfaces."
- Ohmura et al., (US 6,237,046), "Input/Output Control Apparatus Managing Cache Memory Utilizing a Spare Hash Table for Operations if First Hash Table Enters a Synonym State."
- Satoh et al., (US 5,568,628), "Storage Control Method and Apparatus for Highly Reliable Storage Controller with Multiple Cache memories."
- Cochran et al., (US Patent Application Publication 2004/0267959), "Storage System with Link Selection Control."
- Elliott, (US 6,763,409), "Switch-On-The-Fly GBIC Disk Channel Adapter and Disk Channel System."

Conclusion

5. Claims 1-11 are rejected as explained above.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

July 28, 2005

PIERRE BATAILLE
PRIMARY EXAMINER
8/9/05